APPARATUS AND METHOD FOR OVERSAMPLING WITH EVENLY SPACED SAMPLES

ABSTRACT OF THE DISCLOSURE

The architecture and the method of operation of a receiver core are described. The core performs clock and data recovery on an incoming serial data stream transmitted across a wired media, such as a chip-to-chip or card-to-card interconnect. The bit error rate and accuracy of the recovery are optimized without centering of oversampling. Further, random errors due to edge mis-tracking are minimized. The receiver utilizes a phase rotator to detect the edge position of the bits of the data stream, select the optimum data sample and generate early and late signals if the detected edge is not in the expected position. A phase locked loop provides a frequency source for the phase rotator. At least three evenly spaced samples are detected for each bit. A sample processing algorithm, preferably an adaptive behavior algorithm, is used for centering the bit edge between two of the samples.